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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,511	10/03/2003	Antonio Marroig Martinez	10030374-1	1978

57299 7590 06/02/2006

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,511	MARTINEZ, ANTONIO MARROIG	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment dated 5/15/2006.

The applicant has cancelled claims 10 and 24.

The applicant has amended claims 1, 12, 18 and 29.

Claims 1-9 and 11-23 are pending.

Response to Amendment

1. In view of the changes to the drawings FIG. 1-5, the examiner withdraws the objections to said figures and approves entry.

2. In view of the changes to the Specification, paragraphs [0032] and [0038], the examiner withdraws the objections to said paragraphs.

3. The examiner maintains the objection to the Specification, page 6 line 24 as outlined in the previous office action on page 4 which corresponds to paragraph [0029] in the applicant's amendment, for not properly describing the control line **40** in FIG. 2. The applicant has instead referenced the line as control line "44", and so the examiner again asks that the line be corrected to recite, "... to control line 44 40 for ...".

4. In view of the amendments to claims 1, 12, 18 and 21, and the canceling of claim 10, the examiner withdraws all rejections of claims 1, 10, 12, 18 and 21 under 35 USC 112 second paragraph.

5. In view of the canceling of claim 24, the examiner withdraws the rejection of said claim under 35 USC 103.

6. Applicant's arguments with respect to claims 1-9 and 11-23 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Rejections - 35 USC § 103

7. Claims 1-7, 11-15, 18-19 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa, U.S. Patent No. 6977960, and in view of Fan et al. (herein Fan), U.S. Patent Application Publication No. 2004/0030968.

As per claims 1, 12, 18 and 21:

Takinosawa teaches a method based on a built-in self-test circuit for testing a data processing circuit arranged to serialize and deserialize received parallel data into processed parallel data (FIG. 2 39 and 46, and see paragraphs [0022] and [0023] and claim 3), the built-in self-test circuit comprising; a transmit register (FIG. 4a 61 parallel random generator) that transmits parallel data (via FIG. 2 37) to the data processing circuit (FIG. 2 39, 46) for processing the parallel data into processed parallel data (output of FIG. 2 47); a receive register that receives the processed parallel data from the data processing circuit (FIG. 2 48), and an error detector (FIG. 2 49 and FIG. 4b 49) coupled to the receive register for receiving the processed parallel data (by way of FIG. 2 25) and that detects errors in the processed parallel data (FIG.2 4b Comparator 67

yields BIST_ERR), the transmit register (FIG. 4a 61) being a programmable transmit register (via FIG. 4a Data In 21, and Abstract) that transmits parallel data having programmably varying characteristics (Summary, and column 2 lines 35-46). However, Takinosawa has failed to teach or suggest that the comparator is coupled to the transmit register for receiving the transmitted parallel data from the transmit register which is used for comparing to the received processed data. But in the analogous art of Fan, such a feature of comparing the parallel transmitted data to the parallel received data is taught in (see Abstract and FIG. 2 where 64 bit words are compare). And in paragraphs [0012] and [0015] there is stated the benefit of test capabilities of 10 Gbps (as compared to 480Mbps for Takinosawa) for multimode devices such as serializer/deserializers. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to use the features of Fan, including the comparator setup, to improve the test frequency capabilities of Takinosawa for the latest high speed systems.

As per Claims 2 and 22:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 21 wherein the programmably varying characteristics includes data sequence (data patterns of column 8 lines 21-32). And in view of the motivation previously stated, the claims are rejected.

As per Claims 5 and 14:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 12 wherein the programmable transmit register comprises a programmable bit sequence generator

that generates the transmitted data (column 2 lines 35-46 and column 5 lines 64-67 and column 6 lines 1-10). And in view of the motivation previously stated, the claims are rejected.

As per Claim 6:

Takinosawa further teaches the built-in self-test circuit of claim 1 wherein the programmable transmit register comprises a shift register (column 5 lines 64-67 and column 6 lines 1-10). And in view of the motivation previously stated, the claim is rejected.

As per Claims 7, 15 and 19:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 12 or 18 wherein the programmable transmit register comprises a pseudo random counter (column 5 lines 64-67 and column 6 lines 1-10). And in view of the motivation previously stated, the claims are rejected.

As per Claim 11:

Takinosawa further teaches the built-in self-test circuit of claim 1 wherein the error detector comprises a comparator (FIG.4b 67). And in view of the motivation previously stated, the claim is rejected.

As per Claims 3, 4, 13 and 23:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 12 or 21 wherein the programmably varying characteristics include data sequence but fails to disclose varying data length. But Fan does teach this feature in paragraph [0056 And in view of the motivation previously stated, the claim is rejected.

8. Claims 8, 9, 16, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa, U.S. Patent No. 6977960, in view of Fan et al. (herein Fan), U.S. Patent Application Publication No. 2004/0030968 as applied to claims 1, 12 and 21 above, and further in view of Chen et al. (herein Chen), U.S. Patent No. 5726991. Although Takinosawa teaches a pseudo random counter, the reference fails to disclose a register array with pointer. But in the analogous art of Chen, this feature is disclosed in column 3 lines 65-67 and column 4 lines 1-20. Such a read only memory or register is well known in the art and would be considered as an array of registers. A counter or pointer would also be a well-known and obvious part of the data fetch in such a register. And Chen, in column 5 lines 26-32, an advantage is testing of where the transmitters and receivers are one unit, as in a PC. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include with Takinosawa, features of Chen, including fixed pattern data in a read only memory or register, in order to provide test data for testing PC interfaces as well.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings
Examiner
Art Unit 2138

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

All Drawings are approved, 5/23/05 MP

Replacement Sheet

Inventor: Antonio Marriog Martinez
Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD
Attorney: Guy K. Clinger (303) 298-9888
PDNO: 10030374-1

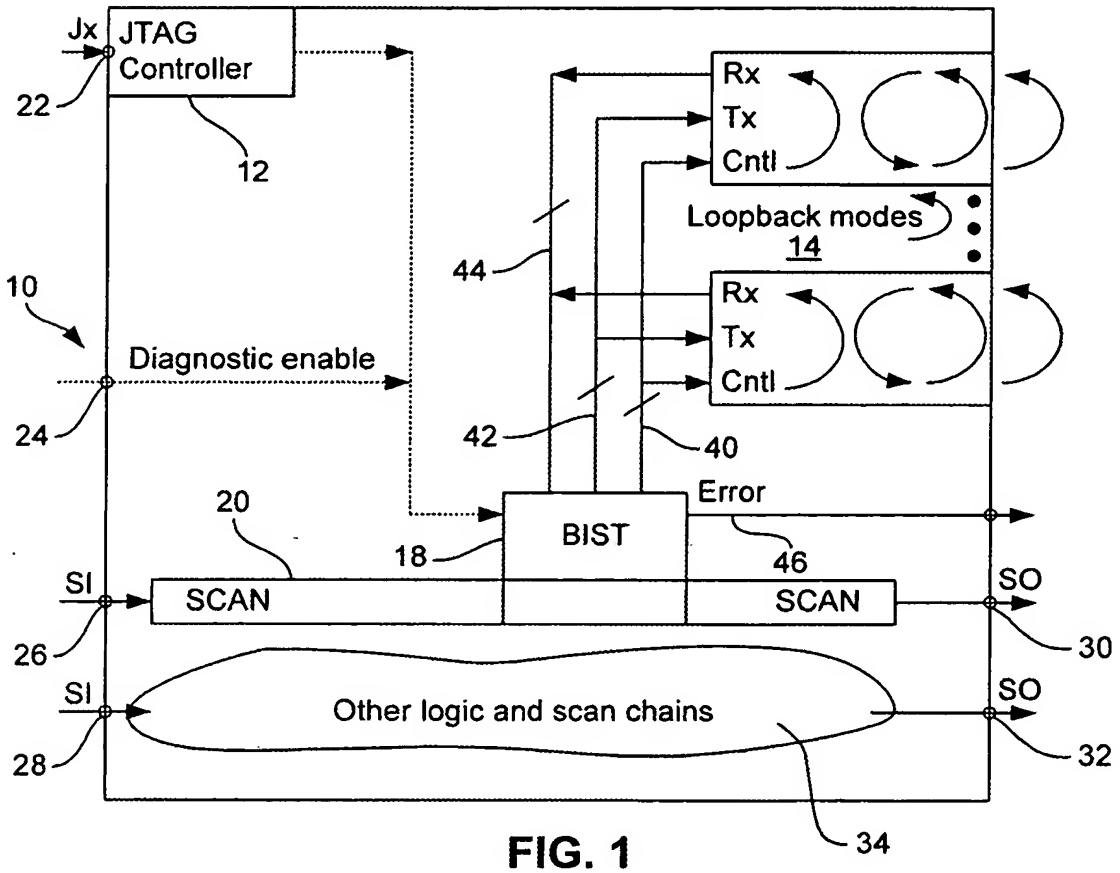

FIG. 1

Inventor: Antonio Marriog Martinez
Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD
Attorney: Guy K. Clinger (303) 298-9888
PDNO: 10030374-1

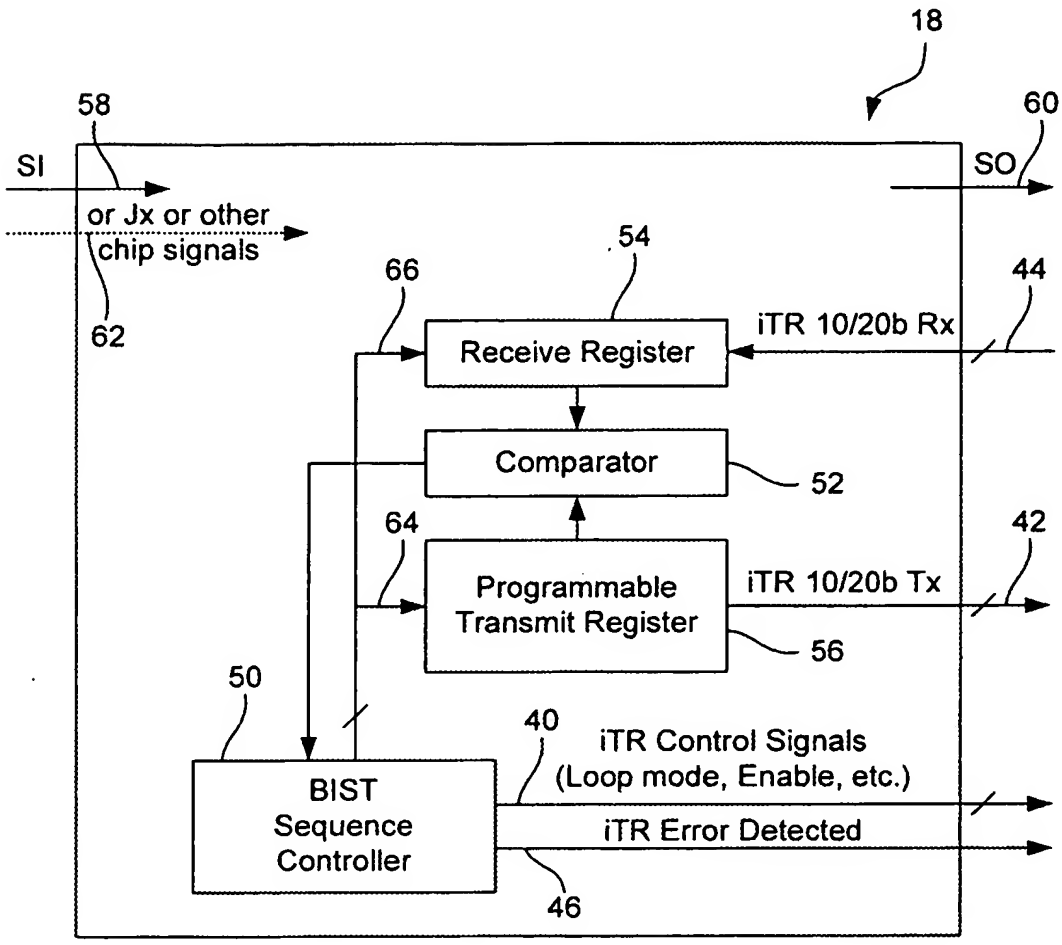

FIG. 2

Inventor: Antonio Marriog Martinez
Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD
Attorney: Guy K. Clinger (303) 298-9888
PDNO: 10030374-1

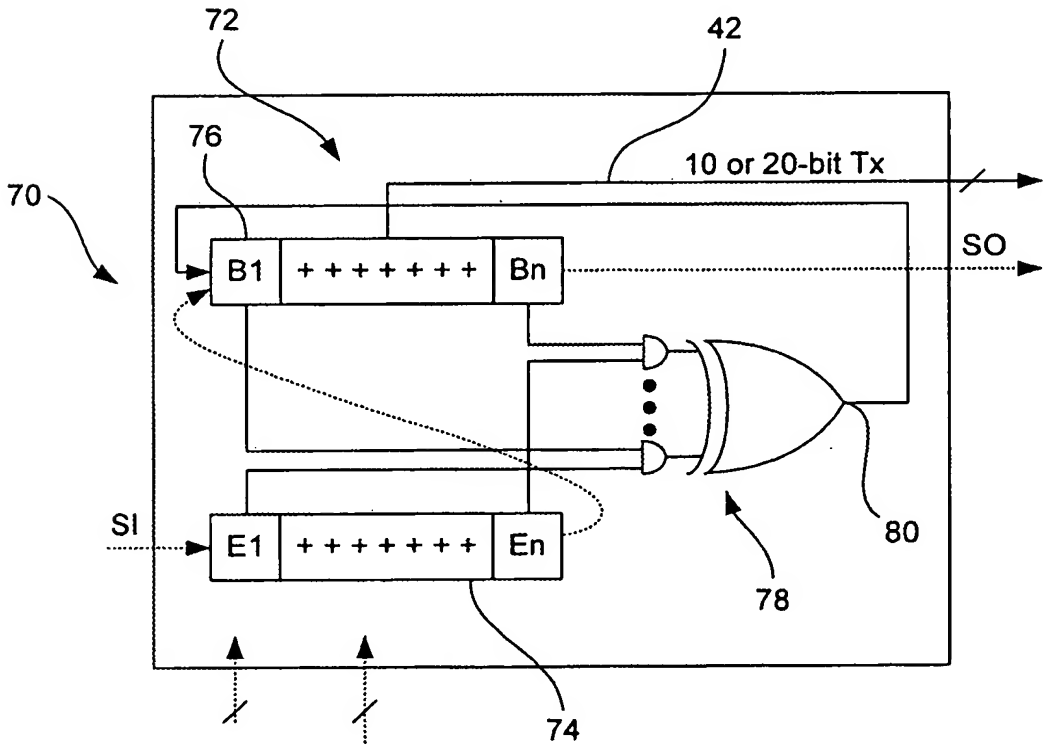

FIG. 3

Inventor: Antonio Marriog Martinez
Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD
Attorney: Guy K. Clinger (303) 298-9888
PDNO: 10030374-1

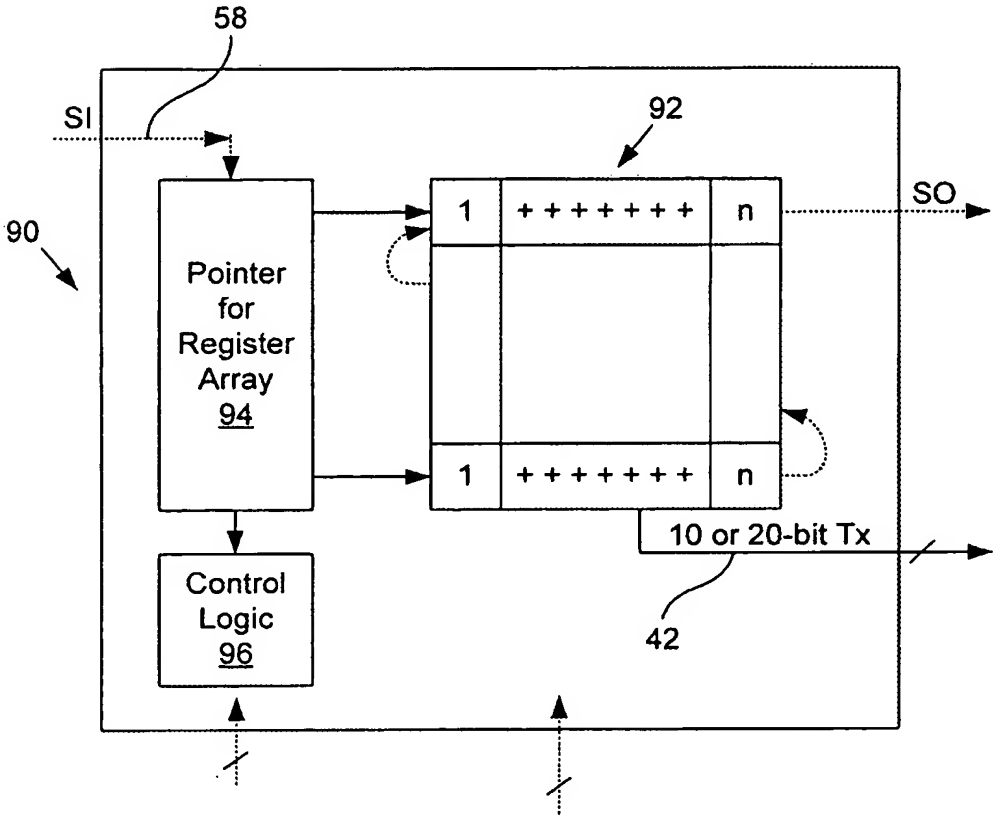

FIG. 4

Inventor: Antonio Marriog Martinez
Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD
Attorney: Guy K. Clinger (303) 298-9888
PDNO: 10030374-1

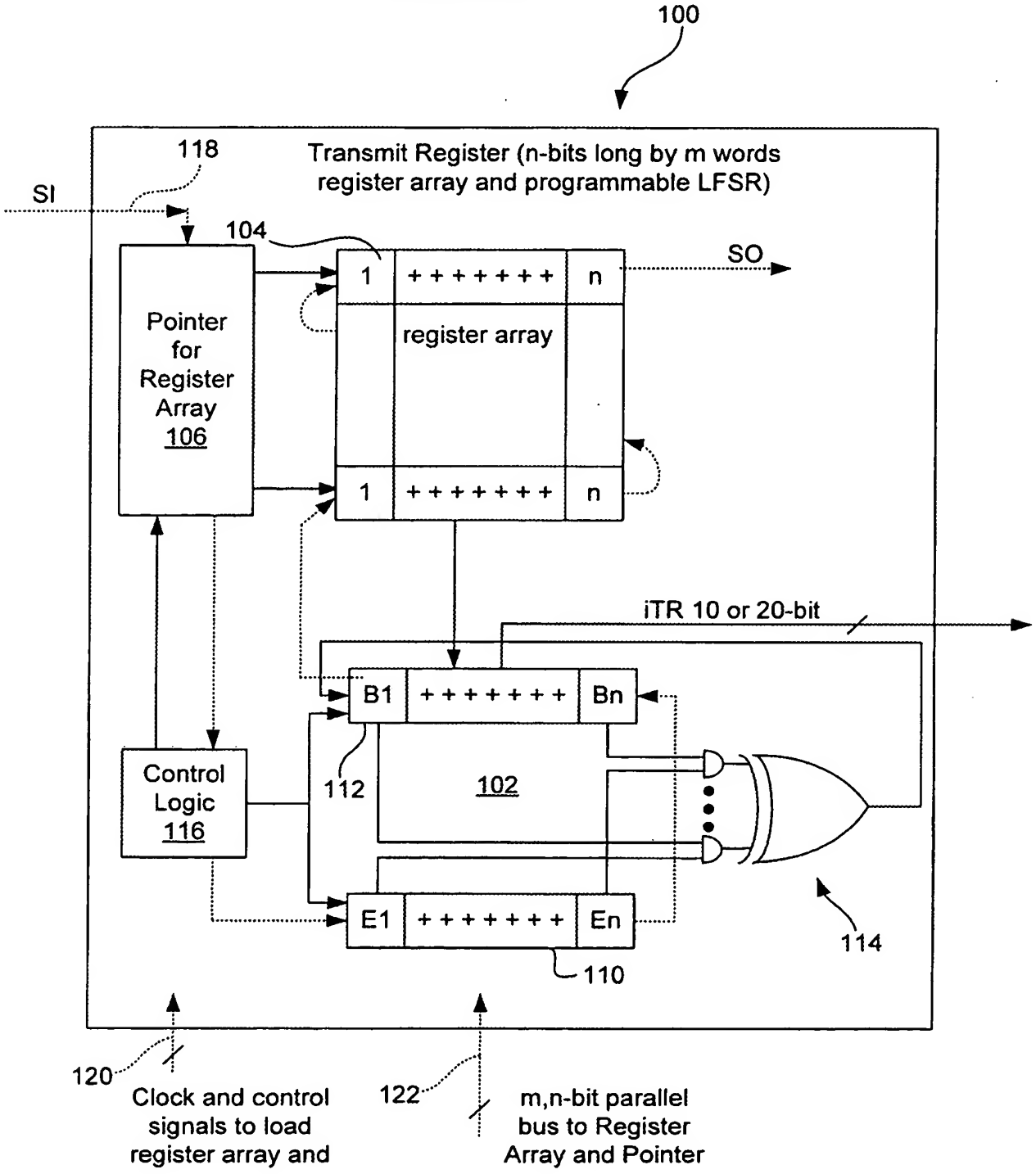

FIG. 5